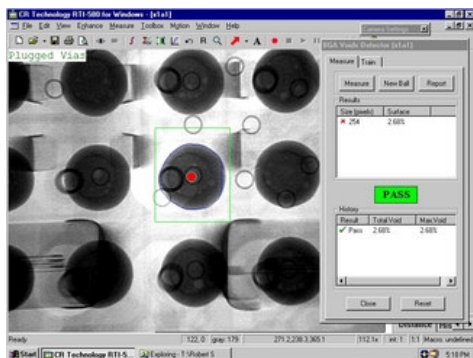


SMT



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Figure 1. Plugged vias.

Vias in SMT Mounting Pads

By Terry Kern, Axiom Electronics

The filling of plated through vias is not an entirely new process, and has been a necessary step to partially filled vias in circuit boards destined to be tested in vacuum fixtures post-assembly. However, these vias were located outside of SMT pads used for mounting components. More recently, as component density increased and lead pitches became smaller, it became difficult or impossible for designers to find sufficient circuit board real estate for connecting SMT mounting pads to discrete conventional vias. It was soon decided that the only feasible option was to move the vias into the pads.

Moving vias into the pads to resolve design problems, however, created other unexpected challenges for both circuit board fabricators and assemblers. It soon was discovered that blind and through vias-in-pad would have to be filled completely and have planar mounting surfaces to avoid defects during assembly, as even small depressions in the mounting pads can lead to solder problems in the finished assembly. The solder problems associated with improper filling of vias-in-pad depends on the amount of filling that actually exists in the via prior to assembly.

A pad with an open through via can have much or all of its solder flow into or through the via hole, resulting in an insufficient solder joint or open. Partially filled through or blind vias associated with component mounting pads will have solder joints with insufficient solder or voids. This is a particular concern under BGAs, as these voids can decrease both the electrical and thermal conductivity of the solder joint, and possibly lead to its mechanical failure. Such defects would require expensive rework and touch up.

Unfortunately, it is not an easy task to properly fill vias to achieve a planar mounting surface in SMT pads. When via filling was needed to draw a vacuum during test, it was felt to be sufficient to plug the vias from one side of the circuit board with standard LPI resists, which only have 60–80% solids content. However, this method was not always completely successful, as occasionally hole plugs would shrink as the solvent in the LPI evaporated, leaving a gap between the plug and the hole wall. This made drawing a vacuum difficult.

Attempts were then made to fill the vias from both sides of the circuit board, but this would trap solvents in the holes, which expanded during solder reflow. The end result was cracked and raised hole plugs that admitted air when subjected to a vacuum during test. Neither of these methods would leave a planar surface satisfactory for mounting purposes on SMT mounting pads containing vias.

With the advent of blind and buried vias, plugging pastes were developed that had nearly 100% solids content. Later, these pastes were used to fill through vias. This change eliminated these solvent problems, and permitted the development of planar surfaces on filled vias. The filling itself could be done with either conductive compounds (e.g. silver-filled epoxy) or

less expensive non-conductive resins, using standard screen-printing techniques. Typically, circuit board holes were filled from one side, and then tack dried prior to filling the holes from the opposite side prior to a final cure. Planarization was done using chemical and/or mechanical polishing of the surface of the circuit board prior to the application of the plated finish on the circuitry.

However, as via holes became smaller, it became more difficult to consistently and completely fill the holes using screen printing. Board suppliers recognized the need for a reliable method of filling via holes; an electroplating process was developed that would fill the holes with copper. After the plating process had been implemented, it was also found that copper-filled vias have advantages over conductive pastes. Not only do they have the same electrical properties as other circuitry on the board, they can improve thermal conductivity and heat dissipation because copper transmits more heat than conductive compounds.

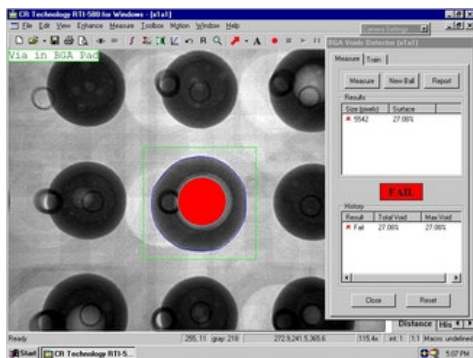
While the use of via-in-pad technology is no longer regarded as an unacceptable way to resolve a design problem, it should only be used if no other options are available. Because of additional steps and material required, the requirement for filling vias adds to the cost of manufacturing the circuit board, and may have a negative effect on yields. In addition, the choice of circuit board fabricators is limited to vendors who indicate that they have the capability of properly filling vias. Proper filling is emphasized, as circuit boards with improperly filled vias will incur additional costs during assembly to correct the problem. Corrective measures required will include identifying and fixing defective vias prior to the application and reflow of solder paste, as well as additional inspection and post-reflow rework to ensure that affected solder joints have sufficient solder.

Finally, if the need to increase density and/or incorporate finer-pitch array packages has dictated that the designer use via-in-pad technology, then documentation should clearly identify this requirement. Circuit board fabrication drawings and data files must identify filled vias, and the drawing should clearly state that the vias must be completely filled, planarized, and plated over with copper and the selected surface finish. Via-in-pad requirements should be discussed with the fabricator, and some assurances given that this process is understood and within their capabilities.

Conclusion

Designers should identify blind and through vias-in-pad that need to be filled; documentation and data files must clearly and unambiguously support this requirement. Fabricators should have the experience and capability to consistently produce circuit boards with properly filled vias-in-pad that are reliable, and will meet the customer's performance objectives. Assemblers should verify that their processes will not degrade the circuit boards, and that the finished assembly will meet the customer's specified requirements. **SMT**

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Figure 2. Example of failed via in BGA pad.

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